REMARKS/ARGUMENTS

The Applicant acknowledges the receipt of the Office Action mailed December 2, 2004. The rejection was a final rejection; accordingly applicant is filing a Request for Continued Examination (RCE) with this amendment. Claims 1-32 are now pending and stand rejected. Reconsideration and allowance of claims 1-22, as amended, is respectfully requested.

I. Rejection of claims 1-32 under 35 U.S.C. 102(b)

Claims 1-32 were rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,727,194 to Shridhar et al. (hereinafter Shridhar).

A. Shridhar repeatedly fetches the repeatedly executed instruction

Claims 2, 3, 9 and 10 have been amended to recite that the single instruction is executed repeatedly without refetching the single instruction and without fetching any other instruction. Claims 1, 8 and 15 recites that the single instruction is executed repeatedly without refetching the single instruction. Fetching, or refetching an instruction entails going across a bus to a main memory to obtain an instruction. The present invention avoids going across a bus by repeatedly executing (re-executing) the instruction latched into the Instruction Register (IR), rather than re-fetching and executing. By contrast, Shridhar is a "pipelined" system that uses a repeat bit. In a pipelined system, a number of instructions are fetched and used to fill an instruction stream that is then executed. This is illustrated in tables 1 and 2 of Shridhar, an examination of which shows that an instruction is being fetched every cycle, such as the instruction being repeated *e.g.*, instr_1, instr_2 in table 1 or instr_a, in Table 2, or another instruction *e.g.*, nop at cycles 2 and N+2 in Table 2. Furthermore, Shridhar teaches, "during cycle N+1 the PC is incremented past cycle N+2. This step completes the *repeated fetching* of instr_a; however, instr_a will be executed twice more in cycles N+2 and N+3 to provide the requisite N iterations of instr_a."(col. 11, lines 37-41, *emphasis added*). Therefore, Shridhar does not teach that a single instruction is executed repeatedly without

refetching the single instruction, nor does Shridhar teach that a single instruction is executed repeatedly without refetching the single instruction and without fetching any other instruction.

A benefit of a system implementing the methodology of the present invention is that it can use a Von Neumann bus, where instruction and data transfer occur on the same bus, as opposed to a Harvard bus, which utilizes separate busses for instruction and data transfer. This is because the present invention does not fetch any instructions while the instruction being repeated is executing. Because the bus is not being used for instruction fetches, the instruction being repeatedly executed can transfer data across the same bus that is used for fetching instructions. For example, an instruction such as Move [data from a 1st memory location],[to a second memory location] can write across the same bus used for fetching instructions at the same as the instruction is executing, thus obviating the need for an additional bus.

Below is a portion of Table 2 of Shridhar showing the Fetch, Decode and Execute registers, the post decode status of the PC register alongside the present invention.

Table 2 of Shridhar					Present invention	
Cycle	F	D	X	PC	F	X
1	instr_a	delay	Repeat	@nop	count	load count
2	nop	instr_a	Delay	@instr_a	repeat	fetch repeat
3	instr_a	nop	instr_a	@instr_a	idle	x-repeat
4	instr_a	instr_a	nop	@instr_a	instr_a	fetch instr_a
5	instr_a	instr_a	instr_a	@instr_a	idle	x-instr_a
6	...		instr_a		idle	x-instr_a
N	...			@instr_a	idle	x-instr_a
N+1	instr_a	instr_a	instr_a	@nop	idle	x-instr_a
N+2	Nop	instr_a	instr_a	@instr_b	Idle	x-instr_a
N+3	instr_b	Nop	instr_a		Idle	x-instr_a
N+4		instr_b	nop		instr_b	fetch instr_b

N+5			instr_b			

* x-repeat is when the repeat instruction is executed, and x-instr_a denotes cycles when instr_a is being executed.

Note that Shridhar fetches instr_a during cycles 1, 3-5 and N+1. Furthermore, during cycles 2 and N+2, Shridhar fetches the nop instruction, which is not needed by the present invention.

Claims 4-7, 11-14 and 16-32 are directly dependent from one of claims 1, 2, 3, 8-10 and 15 and therefore contain each and every element of one of these claims . Therefore, for the reasons just set forth for claims 1, 2, 3, 8,-10 and 15, claims 4-7, 11-14 and 16-32 are also not anticipated by Shridhar.

B. Shridhar does not stall the program counter

In addition to the reasons set forth above, claims 2, 3, 6, 9, 10, 13, 15, 20 and 25-32 recite that the program counter is effectively stalled (*e.g.*, does not move) until either the value in the register is less than or equal to zero or the single instruction has been executed for as many times as indicated by the count value. By contrast, Shridhar does not stall the program counter, but instead "must first assemble the code fragment into a sequence of executable instructions 128d-1, which are then loaded into the primary memory (col. 8, lines 1-3) because "all of the instructions are held in contiguous memory locations so they can be sequentially fetched by simply incrementing the PC address 145 supplied to the fetch stage 112" (col. 8, lines 13-16). Therefore, for the reasons just set forth, claims 2, 3, 6, 9, 10, 13, 15, 20, 25-32 are not anticipated by Shridhar.

II. Conclusion

In summary, Applicant respectfully submits that all pending claims are novel and non-obvious over the prior art of record. Reconsideration and allowance of all pending claims are therefore respectfully requested. If the Examiner believes there are any further matters that

need to be discussed in order to expedite the prosecution of the present application, the Examiner is invited to contact the undersigned.

If there are any other fees necessitated by the foregoing communication, please charge such fees to our Deposit Account No. 50-0902, referencing our Docket No. (72255/02662).

Respectfully submitted,

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